REMARKS

By the forgoing amendments, claims 16-24, 27, 28 and 30 have been amended, and claims 1-15 have been canceled, without prejudice. Thus, claims 16-30 currently are pending and are subject to examination in the above-captioned patent application. No new matter is added by the forgoing amendments, and these amendments are fully supported by the specification. Applicants respectfully request that the Examiner reconsider the above-captioned patent application in view of the foregoing amendments and the following remarks.

The Examiner objects to the title of the invention as being non-descriptive of the claimed invention. Applicants have amended the title of the invention and submit that the replacement title of the invention is descriptive of the claimed invention. Therefore, Applicants respectfully request that the Examiner withdraw the objections to the title of the invention.

The Examiner notes that the above-captioned patent application does not include an abstract of the disclosure. Applicants have amended the above-captioned patent application to include an abstract of the disclosure. Therefore, Applicants respectfully request that the Examiner withdraw the objections to the abstract of the disclosure.

The Examiner also objects to the arrangement of the specification as allegedly not including proper headings for each section of the application. In response to the Office Action mailed February 24, 2004, on July 26, 2004, Applicants submitted a substitute specification in accordance with 37 C.F.R. § 1.121(b), which included

appropriate headings for each section. Therefore, Applicants respectfully request that the Examiner withdraw the objections to the specification.

Moreover, the Examiner objects to the drawings to as including reference numerals not mentioned in the specification. Applicants have amended figure 4 to replace the reference numeral 251 with the reference numeral 115, and have amended the specification to mention reference numerals 107 and 302. Therefore, Applicants respectfully request that the Examiner withdraw the objections to the drawings.

The Examiner objects to claims 16, 17, 19, 21, 22, and 30 as allegedly including informalities. Applicants have amended claims 16, 17, 19, 21, 22, and 30 in accordance with the Examiner's suggestions. Therefore, Applicants respectfully request that the Examiner withdraw the objections to claims 16, 17, 19, 21, 22, and 30.

The Examiner also rejects claims 16-30 under 35 U.S.C. § 112, ¶2, as allegedly being indefinite. Applicants have amended claims 16 23, 27, 28, and 30 to correspond to the Examiner's understanding of the claimed invention, as set forth in paragraphs 15-22 of the Office Action. Therefore, Applicants respectfully request that the Examiner withdraw the indefiniteness rejection of claims 16-30.

Moreover, the Examiner rejects claims 16-18, 21-27, and 29 under 35 U.S.C. § 102(e), as allegedly being anticipated by U.S. Patent No. 6,298,434 to Lindwer. Applicants respectfully traverse this anticipation rejection, as follows:

Java is an example of a Virtual Machine Language which is designed to run on a so-called Java Virtual Machine (JVM). The JVM defines an 8-bit instruction set - each

instruction is called a "bytecode". In practice, JVMs are emulated using processors such as Pentium™ processors. This requires a translation to be made between the 8 bit Java instructions and the 32 bit instructions used by Pentium processors.

The starting point for the present invention is a desire to provide a low cost, but still efficient, Java based microprocessor, such as might be used in extremely low cost applications. This means that the memory requirements are relatively low, and the architecture may be relatively simple. In known systems, it has been proposed to achieve relatively low memory requirements by designing a microprocessor which directly executes Java bytecode, i.e., the microprocessor has a physical structure and mode of operation corresponding to a JVM. However, many of the JVM instructions are very costly to implement in hardware. This means that such a Java processor must either be complex (costly) or it must implement some of the complicated JVM instructions via a subroutine mechanism (which carries a speed penalty).

In order to reduce the overheads of implementing Virtual Machine bytecode, such as JVM instructions, the inventors of the present invention have recognized that it is advantageous to first transform the Virtual Machine bytecodes into 8 bit instructions which have a structure which allows directly executable (simple) instructions to be easily distinguishable from instructions which are implemented by a subroutine call (the translation between the Virtual Machine bytecodes and the 8 bit instructions is easily achieved using for example a one-to-one mapping mechanism). While the translation step itself involves some processing overheads, this is more than compensated for by

the fast subroutine call mechanism which translation facilitates. It is *at least* the operation on **translated** 8 bit instructions which distinguishes the claimed invention from the known architectures for executing Virtual Machine bytecode.

The Examiner asserts that Lindwer discloses or suggests a microprocessor system having all of the features defined in claim 16 of the present application. In particular, the Examiner asserts that Lindwer teaches a microprocessor system for executing Virtual Machine bytecodes which have been translated into respective 8-bit microprocessor instructions. However, Applicants respectfully disagree with the Examiner's asserts, and submit that Lindwer does not disclose or suggest a microprocessor system for executing Virtual Machine bytecodes which have been translated into respective 8-bit microprocessor instructions, as set forth in independent claim 16.

Specifically Lindwer teaches a processor core plus a pre-processing unit for translating Virtual Machine bytecodes (Java) into instructions which can be directly executed by the processor core. It is stated in column 4, lines 36 to 38, that the processor core may be a RISC-type core of the MIPS type. Such processors all use a 32-bit instruction set. The pre-processor of Lindwer therefore converts 8-bit JVM bytecodes into 32-bit RISC instructions. It is not the case that Lindwer discloses or suggests a microprocessor system for executing Virtual Machine bytecodes which have been translated into respective 8-bit microprocessor instructions.

In particular, the Office Action refers repeatedly to the "8-bit" instructions described in Lindwer as corresponding to the 8-bit instructions referred to in claim 16. However, **the only 8-bit instructions of Lindwer are the JVM bytecodes**. The 8-bit instructions of claim 16 **are not the Virtual Machine bytecodes, but rather are the translated Virtual Machine bytecodes**. This is a very significant point. As already highlighted above, JVM instructions can be costly to implement in a dedicated JVM processor. By first translating the JVM instructions into 8-bit bytecodes which are more easily executable (translation may be done offline, e.g. by a suitable "compiler" program, or on-the-fly during execution of a JVM program), a cheaper and more efficient microprocessor can be produced. Therefore, Applicants respectfully request that the Examiner withdraw the anticipation rejection of independent claim 16.

Claims 17, 18, 21-27, and 29 depend from independent claim 1. Therefore, Applicants respectfully request that the Examiner withdraw the anticipation rejection of claims 17, 18, 21-27, and 29.

The Examiner rejects claims 19, 20, and 28 under 35 U.S.C. § 103(a), as allegedly being rendered obvious by Lindwer in view of various other references. However, claims 19, 20, and 28 depend from independent claim 16, and for the reasons set forth above, Applicants submit that independent claim 16 is allowable. Therefore, Applicants respectfully request that the Examiner withdraw the obviousness rejection of claims 19, 20, and 28.

The Examiner rejects independent claim 30 under 35 U.S.C. § 103(a), as allegedly being rendered obvious by Lindwer in view of U.S. Patent No. 4,937,783 to Lee and further in view of U.S. Patent No. 5,937,193 to Evoy. Specifically, the Examiner asserts that in Lindwer, "special virtual machine instructions are simply converted and sent to the processor core for execution," and that "there must be means for analyzing the virtual machine instructions to determine what type they are." Applicants respectfully disagree with the Examiner's assertion.

In particular, in Lindwer, the special virtual machine instructions are not simply converted and sent to the processor core for execution. Instead, the pre-processor of Lindwer comprises intelligence which analyses the JVM program as a whole to see if sections of that code are best executed using subroutines. Secondly, the pre-processor of Lindwer does not analyze the JVM instructions to determine what type they are. Specifically, **JVM instructions do not have a type in respect of whether they correspond to fixed or user defined operations**. More specifically, Lindwer does not detect the presence of a distinguished bit to determine type because **such a bit is not present in JVM instructions**. Therefore, Applicants respectfully request that the Examiner withdraw the obviousness rejection of claim 1.

CONCLUSION

Applicants respectfully submit that the above-captioned patent application is in condition for allowance, and such an issuance of a Notice of Allowance are earnestly solicited. Should the Examiner determine that any further action is necessary to place this application into better form, the Examiner is encouraged to telephone the undersigned representative at the number listed below. Applicants believe that no fees are due as a result of this submission. Nevertheless, in the event of any variance between the fees determined by Applicants and those determined by the U.S. Patent and Trademark Office, please charge any such variance to the undersigned's Deposit Account No. 01-2300.

Respectfully submitted,

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Enclosures: Figure 4 (Replacement and Marked-Up Copy)

Amendments to the Drawings:

The attached drawing sheet includes changes to Figure 4. Specifically, Applicants have amended figure 4 to place the reference numeral 251 with the reference numeral 115

Attachments: Replacement drawing sheet

Annotated drawing sheet showing the changes to Figure 4.

Annotated Marked-up Drawings
Response to February 24, 2004 Office Action
Serial No.: 09/806,490

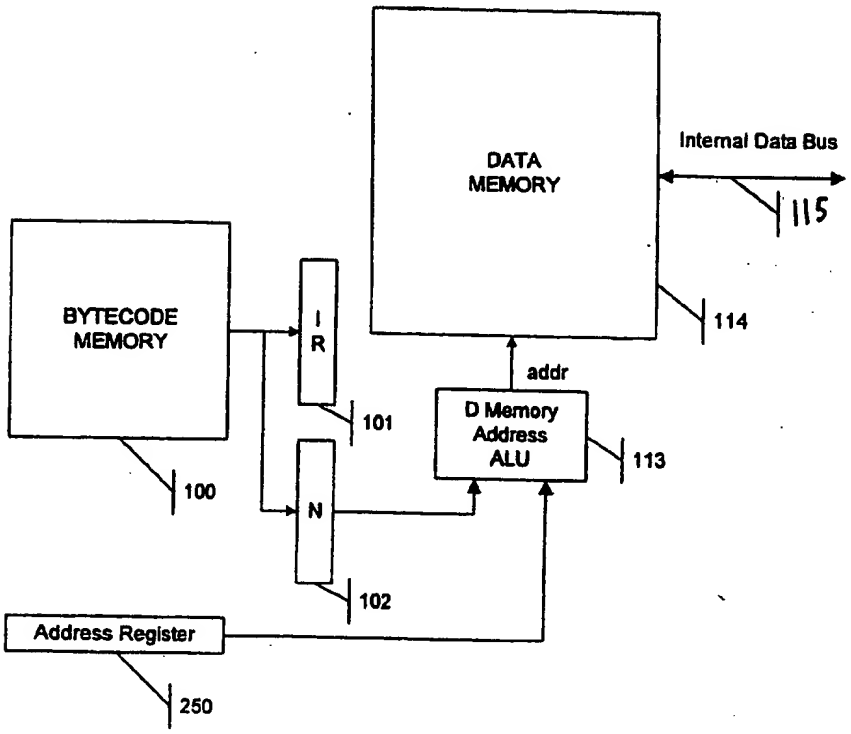

Figure 4